ERROR CORRECTING LOGIC SYSTEM

Abstract

The invention includes an error correcting logic system that allows critical circuits to be hardened with only one redundant unit and without loss of circuit performance. The system provides an interconnecting gate that suppresses a fault in one of at least two redundant dynamic logic gates that feed to the interconnecting gate. The system is applicable to dynamic or static logic systems. The system prevents propagation of a fault, and addresses not only soft errors, but noise-induced errors.